a second capping layer in communication with at least a portion of said gate and said drain;

a second portion of said gate oxide region in communication with at least a portion of said gate and said drain;

said drain, said gate, said second capping layer, and said second portion of said gate oxide region defining a second gap therein, said second gap having one of a gas and a vacuum therein, wherein no dielectric material is positioned between said second gap and any one of said gate, said drain, said second capping layer, and said second portion of said gate oxide region; and

a second implant junction area located in said substrate assembly beneath said second gap and extending partially beneath said gate and said drain, wherein said second junction area includes a pocket implant junction.

C3 Cont.

REMARKS

Remarks Concerning Present Response

In the present response, Applicants have amended claims 17, 125, and 128. In addition, Applicants have canceled claim 29, 30, 104-112, 114-117, 119, 120, 122, and 123. Claims 17, 19, 98-103, 125, 126, and 128 are now pending in the subject application.

Remarks Concerning Response Dated July 18, 2002

In the office action dated October 2, 2002, it was stated that "[t]he amendment filed on 7/18/02 (in response to an office action dated March 18, 2002) amends all pending claims to read on a non-elected invention and thus is non-responsive" (see page 2 of October 2, 2002 office

action). Applicants do not concede the correctness of the Examiner's position as set forth in either the March 18, 2002 office action or the October 2, 2002 office action. Nonetheless, to expedite prosecution of the subject application, Applicants have herein canceled claims 29, 30, 104-112, 114-117, 119, 120, 122, and 123, without prejudice or disclaimer to the subject matter contained therein.

Upon entry of the present amendment, Applicants submit that the pending claims read on the elected invention, and thus the present response, coupled with the arguments set forth in the response dated July 18, 2002, constitute a responsive reply to the office action dated March 18, 2002. Applicants also respectfully request that the Examiner consider the July 18, 2002 response in connection with the present amendment.

Declaration Under 37 C.F.R. §1.131

Enclosed is a Declaration under 37 C.F.R. §1.131 ("Declaration") concerning the parent application (Serial No. 09/144,662) of the subject application and Exhibits A - J that support, accompany and form part of the Declaration in conformance with 37 C.F.R. §1.131.

The Declaration has been executed by Fernando Gonzalez and Chandra Mouli, joint inventors for both the parent application and the subject application, and is submitted herewith to overcome the previously cited Wu reference (U.S. Patent No. 5,977,561 - filing date March 2, 1998). The Declaration establishes conception of the invention prior to the effective date of the Wu reference and due diligence from prior to the effective date of the Wu reference to the filing date of the parent application. Applicants submit that because the subject application is a divisional patent application of the parent application, the Declaration concerning the parent application also establishes, for at least the claims in the subject application that were rejected under 35 U.S.C.

§102(e) as being anticipated by Wu, conception prior to the effective date of the Wu reference and due diligence from prior to the effective date of the Wu reference to the filing date of the subject application.

Applicants further submit that the Declaration is not an admission that the claims of the subject application read on the references cited by the Examiner. Submission of the Declaration is merely to expedite prosecution, in contrast to further arguing what Applicants deem to be allowable subject matter. Therefore, in view of the Declaration, Applicants request that the rejections of claims 17, 125, and 128 under 35 U.S.C. §102(e) as being anticipated by Wu, and the rejections of claims dependent therefrom, be withdrawn.

CONCLUSION

Applicants respectfully request issuance of a Notice of Allowance for the subject application. If the Examiner is of the opinion that the subject application is in condition for disposition other than allowance, the Examiner is respectfully requested to contact Applicants' attorney at the telephone number listed below, in order that the Examiner's concerns may be expeditiously addressed.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims

The claims have been amended as follows:

17. (Twice Amended) A transistor formed on a substrate assembly, comprising:

a raised drain structure;

a raised source structure;

a gate located between said source and said drain;

a first capping layer in communication with at least a portion of said gate and said source;

a first portion of a gate oxide region in communication with at least a portion of said gate and said source;

said source, said gate, said first capping layer, and said first portion of said gate oxide region defining a first gap therein, said first gap having one of a gas and a vacuum therein, wherein no dielectric material is positioned between said first gap and any one of said gate, said source, said first capping layer, and said first portion of said gate oxide region;

a first implant junction area located in [a] said substrate assembly beneath said first gap and extending partially beneath said gate and said source;

a second capping layer in communication with at least a portion of said gate and said drain;

a second portion of [a] said gate oxide region in communication with at least a portion of said gate and said drain;

said drain, said gate, said second capping layer, and said second portion of said gate oxide region defining a second gap therein, said second gap having one of a gas and a vacuum therein, wherein no dielectric material is positioned between said second gap and any one of said gate, said drain, said second capping layer, and said second portion of said gate oxide region; and

a second implant junction area located in [a] said substrate assembly beneath said second gap and extending partially beneath said gate and said drain.

125. (Twice Amended) A transistor formed on a substrate assembly, comprising:

a raised drain structure;

a raised source structure;

a gate located between said source and said drain;

a first capping layer in communication with at least a portion of said gate and said source;

a first portion of a gate oxide region in communication with at least a portion of said gate and said source;

said source, said gate, said first capping layer, and said first portion of said gate oxide region defining a first gap therein, said first gap having one of a gas and a vacuum therein, wherein no dielectric material is positioned between said first gap and any one of said gate, said source, said first capping layer, and said first portion of said gate oxide region;

a first implant junction area located in [a] said substrate assembly beneath said first gap and extending partially beneath said gate and said source, wherein said first junction area includes doped silicon areas;

a second capping layer in communication with at least a portion of said gate and said drain;

a second portion of [a] said gate oxide region in communication with at least a portion of said gate and said drain;

said drain, said gate, said second capping layer, and said second portion of said gate oxide region defining a second gap therein, said second gap having one of a gas and a vacuum therein, wherein no dielectric material is positioned between said second gap and any one of said gate, said drain, said second capping layer, and said second portion of said gate oxide region; and

a second implant junction area located in [a] said substrate assembly beneath said second gap and extending partially beneath said gate and said drain, wherein said second junction area includes doped silicon areas.

128. (Twice Amended) A transistor formed on a substrate assembly, comprising:

a raised drain structure;

a raised source structure;

a gate located between said source and said drain;

a first capping layer in communication with at least a portion of said gate and said source;

a first portion of a gate oxide region in communication with at least a portion of said gate and said source;

said source, said gate, said first capping layer, and said first portion of said gate oxide region defining a first gap therein, said first gap having one of a gas and a vacuum therein, wherein no dielectric material is positioned between said first gap and any one of said gate, said source, said first capping layer, and said first portion of said gate oxide region;

a first implant junction area located in [a] said substrate assembly beneath said first gap and extending partially beneath said gate and said source, wherein said first junction area includes a pocket implant junction;

a second capping layer in communication with at least a portion of said gate and said drain;

a second portion of [a] said gate oxide region in communication with at least a portion of said gate and said drain;

said drain, said gate, said second capping layer, and said second portion of said gate oxide region defining a second gap therein, said second gap having one of a gas and a vacuum therein, wherein no dielectric material is positioned between said second gap and any one of said gate, said drain, said second capping layer, and said second portion of said gate oxide region; and

a second implant junction area located in [a] said substrate assembly beneath said second gap and extending partially beneath said gate and said drain, wherein said second junction area includes a pocket implant junction.